

Key Ideas, Formulas, Procedures in EECS 42

Lecture 1: Electrical Engineering, signals as voltages and currents, energy flow. Devices and integrated circuits. Analog and digital representations. Electronic building blocks.

Lecture 2: Concepts of charge, electric field, energy, potential, flow (flux or fluence), electric current, power. Scalars and vectors. Ground as reference potential.

Important electrical quantities	SI prefixes	Constants
Electric Field ξ (V/m)	femto f 10^{-15}	$q=1.6 \times 10^{-19}$
Charge Q (C)	pico p 10^{-12}	$\epsilon_0=8.85 \times 10^{-12}$ F/m
Force $Q \times \xi$ (N)	nano n 10^{-9}	
Current I or i (A)	micro μ 10^{-6}	
Potential V or v (V)	milli m 10^{-3}	
$P=IXV$ (W) Power flows in for associated signs	kilo k 10^3	
Force \times distance (QV)= Energy (J)	mega M 10^6	
Resistance (Ω) $\Omega = V/A$	giga G 10^9	
Capacitance (F) $F=Q/V$		
Inductance (H) $H=(V\text{-sec})/A$		

Lecture 3: Resistors and Ohms law. Associated and unassociated sign conventions. Voltage and current sources. Series and parallel combinations of resistors. Wires.

$V = I \times R$ (ohms law)	V and I are associated (I into +V terminal)
$R_1 \parallel R_2 \quad R = R_1 \times R_2 / (R_1 + R_2)$	Parallel resistors
R_1 in series with $R_2 \quad R = R_1 + R_2$	Series resistors
$P = V \times I$ (power flow into element)	V and I are associated (I into +V terminal)

Lecture 4: I-V graphs of two-terminal elements. IV graphs of combinations of elements. Nonlinear circuit elements, Method of Load Lines for solving for I and V.

Lecture 5: Circuits, Nodes, and branches. Kirchoff's Laws (KVL, KCL), Voltage drops, Voltage rises, Node voltages.

Lecture 6: $P=VI$ (positive for power absorbed if signs are associated). Time averaged power is integral of power divided by the interval over which the power is integrated. Computationally, we just sum the area under the $P(t)$ curve and divide by the time interval. For periodic time varying power it is important to integrate over a complete period. For resistors $P(t) = v(t) \times i(t)$ (dissipated as heat). Thus from ohms law $P=V^2/R$ or equivalently I^2R . For a capacitor we know that the energy stored is $1/2QV$ or $1/2CV^2$ since $Q=CV$. We also note that in charging a capacitor from a voltage source (through a resistor) exactly half the energy is wasted (because the Energy delivered by the source is QV).

Lecture 7: All linear single capacitor circuits with resistors have a simple solution for the capacitor voltage: $A + Be^{-t/RC}$. Here R is the effective resistance seen from the terminals of the capacitor (which we will learn how to compute in lectures 8-12). Of course $A+B$ is the initial value and A is the final value. The capacitor voltage cannot jump, that is it cannot change instantaneously.

Lecture 8: The easy method to find the transient waveform is to solve the two DC problems (before and after the transient), and note that the transient is 63% completed after one time constant RC . We sketch the waveform and simply write down the equation. We can shift the time axis of waveforms when the switching event does not occur at $t=0$. Thus if the switch moves at some time t_1 , we plot the transient versus $t-t_1$, rendering the problem identical to the simple case in which the event occurs at $t=0$.

Lectures 9 and 10: Nodal analysis provides a rigorous method of solving circuit problems of arbitrary complexity. An algorithm is used in which the reference and unknown nodes are defined, and KCL is applied at each node and the constitutive relationship of the branch is used to relate the currents in the branches to the node voltages. In the case of floating voltage sources we use a "supernode" enclosing the voltage source and express KCL at this supernode. The simple relationship between the voltages at the two nodes of the supernode provides an auxiliary equation. We can use Nodal analysis to quickly prove the voltage divider formula: V_2 (across R_2) = $V_{tot} \times R_2 / (R_1 + R_2)$ where V_{tot} is the total voltage across the two resistors in series. Similarly we can prove the current divider: I_2 (current through R_2) = $I_{tot} \times R_1 / (R_1 + R_2)$ where I_{tot} is the total current through the two resistors in parallel.

Lecture 11: All linear circuits can be reduced to their Thévenin or Norton Equivalents. If we test the circuit and find its open circuit voltage V_{OC} and short circuit current I_{SC} (associated signs) then the Thévenin voltage source $V_T = V_{OC}$ and the Thévenin resistance R_T equals $-V_{OC}/I_{SC}$. The Norton current source equals $-I_{SC}$ and the Norton resistance is the same as the Thévenin resistance. The resistance may also be found by turning off all the sources and measuring the resistance at the terminals.

Lecture 13: The load line method allows a graphical solution for V and I whenever two circuits with known I - V graphs are connected. If I and V are defined consistently, the solution is simply the intersection of the I - V graphs. Three-terminal or "parametric" I - V graphs provide a means for displaying the I - V characteristics of three-terminal devices (generally with one terminal voltage or current held constant while the I - V graph of the other terminals is plotted). Not all circuits are valid because we can draw circuits which inherently violate KVL (such as when two voltage sources are connected in parallel) or KCL (such as when two current sources are connected in series). Shorting a voltage source or opening a current source is also invalid.

Lectures 14 and 15: Dependent sources provide a mechanism for modeling active devices. Circuits with dependent sources are analyzed the same as with independent sources except that one does not turn off dependent sources in calculation of the Thévenin resistance. Four types of dependent sources exist: Voltage-controlled voltage sources ($V = A_v V_{cd}$), Current-controlled voltage sources ($V = R_m I_c$), Current-controlled current sources ($I = A_i I_c$), and Voltage-controlled current sources ($I = G_m V_{cd}$). The voltage-dependent voltage source is the basis for the linear amplifier model. Real amplifiers have a limited range of linearity; the output saturates when it hits either the upper rail (usually the highest power supply voltage) or the lower rail (the lowest power supply voltage, sometimes ground). Hi-gain amplifiers can be used as comparators or inverters.

Lecture 16: Binary numbers and Boolean algebra provide a description of logic that can be both manipulated mathematically and realized in simple circuit form as logic gates. The most important logic gates: AND (e.g. $F=A \bullet B$), OR (e.g. $F=A+B$), NOT (e.g. $F = \overline{A}$), NAND (e.g. $F = \overline{A \bullet B}$), NOR (e.g. $F = \overline{A + B}$), EXCLUSIVE OR (which is “OR unless AND”). Each of which has its own gate symbol. Two circuits are logically equivalent (identical) if they have the same truth table. DeMorgan’s theorem can transform AND combinations to NOR or OR to NAND: e.g. $A + B = \overline{\overline{A} \bullet \overline{B}}$. Note that distributive properties are valid in Boolean Algebra, but note also that $\overline{A \bullet B} \neq \overline{A} \bullet \overline{B}$ etc.

Lectures 17 and 18: Logic statements or logic equations can be synthesized in straightforward fashion by the following procedure: Write out the truth table for the logic statement. For each “output” in the truth table identify those rows for which the output is true and write an equation “summing” those rows. This Boolean equation may be simplified by eliminating redundancies such as $(A + \overline{A}) = 1$. Then the equation may be implemented with NAND gates by invoking DeMorgan’s theorem to transform it from “OR” to “NAND” form.

Flip-flops are electronic circuits with “memory”; that is they retain their value until an input determines a possible new value. Examples are the S-R flip flop (synchronous or clocked) and the clocked D flip-flop. A proper edge-triggered D flip-flop for example will retain its present output value “Q” until a clock pulse occurs. After a clock pulse Q will take on a new value equal to the logical value of D at the moment of the rising edge of the clock pulse. We can build such flip-flops with logic gates.

Lectures 19 and 20 : The output of actual electronic logic gates are delayed from the input changes because of the time it takes to charge the capacitance on the nodes of the internal circuitry. We define the unit gate delay as the time for the output to become valid after a change in the input (or a clock pulse in the case of synchronous logic). In microprocessor circuits we must allow from 20 to 50 gate delays between clock cycles. If we adopt the simplification that the logic output is valid when the node moves halfway to its final value, then we can say that the unit gate delay is $0.69RC$ where R and C are the resistance and capacitance values associated with the gate delay.

If we have controlled switches, we can build inverters (and logic gates as we will see). With a controlled switch the critical parameter is the resistance, which when combined with the node capacitance will determine the unit gate delay (e.g. $0.69RC$ as above).

The capacitance of each node C, the number of nodes N, the logic voltage V, and the clock frequency f place a lower limit on electronic power in a digital circuit: NCV^2f . Of course if only a fraction α of the gates are being clocked, the power is reduced by the factor α .